# CONFIGURABLE PERIPHERAL DEVICES

## FIELD OF THE INVENTION

**[0001]** The present invention generally relates to data processor systems, and more particularly to a data processor system implemented on a programmable logic device having user selectable peripheral devices.

## BACKGROUND OF THE INVENTION

**[0002]** Microprocessors are one of the most versatile electronic devices used by engineers. Typically, a microprocessor is able to recognize and execute a predetermined set of instructions (e.g., add, compare, subtract, jump, etc.). Engineers can direct a microprocessor to handle different tasks by writing different computer programs using the same set of instructions. As a result, different types of products can use the same microprocessor by changing the associated computer programs.

**[0003]** A microprocessor is typically used with a number of peripheral integrated circuit (IC) devices (such as serial interface, parallel input-output device, interrupt controller, disk drive controller, etc.). In many cases, a microprocessor manufacturer supplies a family of peripheral ICs that works best with its microprocessors. Because microprocessors are used in many types of products, these peripheral ICs also need to be flexible enough to be used in many types of products. This flexibility comes with a price: it is more difficult to use the peripheral ICs and the cost of the extra registers, logic, memory, etc. required to make the peripheral flexible, increases the cost of the peripheral. Another reality of casting peripherals into silicon is that it is extremely difficult to anticipate future changes to standards. If such "future" standards

could be incorporated into a peripheral, the value of the peripheral would be greatly enhanced.

SUMMARY OF THE INVENTION

**[0004]** The above problems can be solved by having a single IC that includes a processor core and one or more peripheral devices selected by a user. Because the peripheral device is configurable, the user can select just the features he/she needs in the IC. As a result, the peripheral devices included in the IC do not have to be flexibly designed in the same manner as commercially available peripheral devices. Consequently, they are easy to use. Because the peripheral device is configurable, the peripheral can be modified over the lifetime of the system. This provides the possibility to adapt to future changes in standards, even after the microprocessor system has been deployed in the field. It also affords the possibility to increase the performance or alter the operation of the peripheral after deployment.

**[0005]** In one embodiment of the present invention, a menu system is used to help the user configure the peripherals and select which peripherals are to be connected to the microprocessor.

**[0006]** The above summary of the present invention is not intended to describe each disclosed embodiment of the present invention. The figures and detailed description that follow provide additional example embodiments and aspects of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0007]** The present invention is illustrated by way of example, and not by way of limitation, in the following figures, in which like reference numerals refer to similar elements.

**[0008]** FIG. 1 is a schematic diagram of an IC containing a configurable processor system of the present invention.

**[0009]** FIG. 2A is a block diagram of a prior art UART.

**[0010]** FIG. 2B is a block diagram of an UART of the present invention.

**[0011]** FIGS. 3A-3C show an exemplary menu system of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

**[0012]** Several examples of configurable peripheral devices will be described. In the following description, numerous specific details are set forth in order to provide a more thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known features have not been described in detail in order to avoid obscuring the present invention.

**[0013]** FIG. 1 is a schematic diagram of an IC 100 containing a configurable processor system of the present invention. IC 100 contains a processor core 104, one or more configurable peripheral devices 106, and an optional RAM 108 attached to processor core 104. Peripheral devices 106 communicate with processor core 104 using a bus 110. Processor core 104 is typically non-configurable, but may also be configurable.

**[0014]** In one embodiment of the present invention, IC 100 is a field programmable gate array that further contains a plurality of input-output (I/O) blocks, such as blocks 122-125, and a plurality of configurable logic blocks (CLBs), such as blocks 127-128. Detail description of these blocks can be found in "The Programmable Logic Data Book 2000," Chapter 3, published by Xilinx, Inc, the content of which is incorporated herein by reference. These blocks can be used to build other circuits that may be connected to the system of the present invention.

**[0015]** The present invention allows a user to include one or more peripheral devices in IC 100. In this invention, a peripheral device is defined as a circuit that (a) delivers

signals to a device external to IC 100 in response to commands by processor core 104 and (b) receives signals from the external device and delivers the signals (sometimes in a modified form) to processor core 104. Examples of peripheral devices are universal asynchronous receiver transmitter (UART), parallel port interface, Ethernet interface, flash memory controller, etc. In the present invention, these peripheral devices can be tailor-made to meet the needs of the users. As an example, consider a prior art UART 160 of FIG. 2A. It contains a microprocessor bus interface unit 162 that is connected to a microprocessor. It also contains a baud rate generator 164 and an associated baud rate register 166. A user can control the baud rate of UART 160 by writing to register 166. UART 160 contains a receiver-transmitter (RX-TX) 168 that receives and sends serial data at the selected baud rate to an external modem (not shown). In order to enhance the performance of UART 160, a FIFO buffer 170 is used to temporarily store the data. UART 160 also contains a modem control signal generator 172 that generates standard control signals, such as the RTS and CTS signals.

**[0016]** Prior art UART 160 is designed to serve general engineering usage. As a result, it includes baud rate register 166 and associated control logic to allow users to easily change the baud rate of UART 160. In the present invention, a user may only need to use a single baud rate, and there is no need to include register 166 and associated logic. As a result, the complexity of the design is reduced. FIG. 2B shows an UART 160a of the present invention that does not contain register 166. Elements common in FIGs. 2A and 2B use the same reference numerals. UART 160a contains a bus interface 162a that can communicate with processor core 104. A baud rate generator 164a, designed to generate a single baud rate, is implemented in UART 160a.

**[0017]** It should be noted that other peripheral devices may be configured using the same principle to reduce the complexity of the design.

**[0018]** The user can select his/her design choices using a menu system. FIG. 3A shows a menu 230 that allows a user to select from a UART, Ethernet controller or flash controller as a target peripheral. Note that the user may select more than one peripheral. Assuming that the user selects a flash controller, a second menu 232 (FIG. 3B) allows the user to select 16-bit, 32 bit and error correction code (ECC) designs. If the user selects ECC, another menu 234 (FIG. 3C) allows the user to select one of several codes. After all the information is entered, a VHDL file will be generated to implement the design. Note that the choices shown in FIGs. 3A-3C are listed as examples only, and various choices can be implemented to meet the needs of users, and the method of implementing the design is not limited to VHDL.

**[0019]** Those having skill in the relevant arts of the invention will now perceive various modifications and additions which may be made as a result of the disclosure herein. Accordingly, all such modifications and additions are deemed to be within the scope of the invention, which is to be limited only by the appended claims and their equivalents.